REMARKS/ARGUMENTS

Claims 1-30 are pending in the present patent application. Claims 1-15, 19-22, and 25-30 stand rejected under 35 USC 103(a) in view of U.S. Patent 5,970,005 issued to Yin (Hereinafter Yin). Claims 23 and 24 are allowed. Applicants have submitted a request for continued examination with this response. By this amendment, claims 1, 3-4, 6, 10-11, 13, 19, 25, and 27-29 have been amended, leaving claims 1-15, 19-22, and 25-30 pending examination. No new matter has been added. Reconsideration of the claims is respectfully requested.

Summary of the Interview with the Examiner

Applicant would like to thank the Examiner for the phone interview conducted July 11, 2005. During the interview, Counsel for Applicants proposed using the terms multiplexing circuit, selection circuit, and the like, being operated by the first address bits for selecting, for example, the second word line. The Examiner agreed that using the terms of art such as selection circuit or multiplexing circuit in this manner clarifies the claims.

Counsel for Applicants notes that the purpose of the interview was for expediting allowance of the patent application. Upon reflection, Applicants believe that, for example, the term "first address bits selecting a second word line" is proper without the term selection circuit as there are many equivalent ways of using the address bits to select the word lines. A selection circuit represents one example, among many examples, of ways to select the second word line using the first address bits.

35 USC §103 Rejections

Claims 1, 10, 19, 25, and 29

In view of Yin, the Office Action has rejected claims 1 and 10 as not stating that the address bits in row registers select a first column of memory using multiplexers, and rejected claim 19 stating Yin discloses a structure and a method for testing, programming, and

verification of a PLD. Further, the Office Action rejected claim 25 as not state shifting programming data into the shift register as the same time that the verification data is shifted out, and rejected claim 29 for obviousness additionally in view of conventional latch circuitry. Applicants respectfully traverse the rejections.

Yin teaches a fundamentally different system and process for programming and verifying data in a programmable integrated circuit as described in the specification and is therefore distinguished from the claimed system and process in a number of respects. For example, in one respect, Yin discloses loading new address bits *each time data is loaded into a memory column* in programming mode and *each time data is read out of a memory column for verification* (Yin, at col. 11, line 36 - col. 12, line 24 and Figures 14-15). In contrast, in one example the present invention is directed at a process that requires less operations than Yin by using a selection circuit responsive to the first address bits (used to select a first word line) to also select a second word line, and loading the first data bits into second memory cells that are part of the second word line. The claimed process reduces the number of times the word line address bits are loaded into the row shift registers, because *one set of address bits* e.g., *first address bits*, are used to load data into a first column of memory *and* to read data out of a second column of memory, e.g., *second memory cells*. For example, claim 1 as amended recites in part "selecting, by a selection circuit responsive to the first address bits, a second word line," claim 10 recites in part "when the second row is selected by the first address bits via the selection circuit," claim 19 recites in part "means for selecting using the first address bits," and claim 25 recites in part, "selecting a second word line using a second selection operation using the first address bits." These elements, among others, are supported in the specification as filed. For example, referring to Figure 2B of the present application, address bits in row registers 621 select a first column of memory using multiplexers 652. After the first column of memory is selected, first data bits are loaded from the first column of memory to column registers 620. The same address bits in row registers 621 also select a second column of memory using multiplexers 652. After the second column of memory is selected, second data bits are loaded into the second column of memory from column registers 620. In conclusion, Yin does not disclose or suggest

selecting a second word line by using a selection circuit responsive to the first address bits to select a second word line.

Claim 29 recites in part "the second row of memory cells are in a second word line selected by the selection circuit responsive to first address bits," and "wherein the first data bits are shifted out of the first registers while second data bits are shifted into the first registers." Yin does not disclose or suggest *selecting a second row of memory cells using first data address bits* and then *shifting data bits into the register at the same time that second data bits are shifted out* of the register (Yin, col. 11 line 36, col. 12 line 24, and Figures 14-15).

Thus, claims 1, 10, 19, 25, and 29 are patentably distinguished over Yin for at least the above reasons.

Dependent claims 2-9, 11-18, 20-22, 26-28, and 30

Claims 2-9 depend from amended claim 1 and are therefore patentable for at least the reasons discussed in relation to claim 1. These claims, however recite additional elements that further distinguish over the cited art. For example, Yin does not teach additional elements recited in claim 2 such as "storing the first data bits using a first set of latches after the first data bits are shifted into the first registers," as recited in claim 5 "loading a first subset of the second data bits that have a first logic state from the first memory cells into the first registers in response to a first verify control signal, and loading a second subset of the second data bits that have a second logic state from the first memory cells into the first registers in response to a second verify control signal," and as recited in claim 7 "shifting the second data bits out of the first registers while shifting third data bits into the first registers."

Yin does not disclose additional elements as recited in amended claim 11 such as "each of the first registers is coupled to two rows of the memory cells", nor as recited in claims 12-14 "each of the second registers is coupled to a first latch that stores the second data bits before the second data bits are programmed into the second row of the memory cells." Further, Yin does not disclose or suggest as recited in claim 15 an "ISC control block that provides a program signal and a verify signal and, as recited in claims 16-18, "wherein second address bits

stored in the first registers select the second row of the memory cells and a third row of the memory cells."

Yin does not teach or suggest additional elements as recited in claim 20 such as a "means for verifying a first subset of the first data at a first logic state, and means for verifying a second subset of the first data at a second logic state," nor as recited in claim 21 "a first register coupled to the first and second rows of memory cells through a multiplexer, the first address bits are stored in the first register for selecting the first row and the second row of memory cells using the multiplexer," nor as recited in claim 23 "each of the second registers storing the second data in latches before the second data is programmed into the second row of memory cells." Yin does not teach or suggest as recite in claim 26 "shifting fourth data bits into the first registers *while* shifting the first data bits out of the first registers," nor as recited in amended claim 27 and claim 28 "selecting, via a selection circuit, the second word line with the first address bits in the second registers," nor as recited in claim 30 "wherein the first row of the memory cells and the second row of the memory cells are selected by address bits in second registers."

Dependent claims 2-9, 11-18, 20-22, 26-28, and 30 are therefore patentably distinguished over Yin. Accordingly, withdrawal of the rejection of claims 2-9, 11-18, 20-22, 26-28, and 30 is respectfully requested.

Allowable Subject Matter

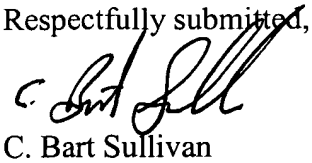
The Office Action indicated that claims 16-18, contain allowable subject matter and claims 23-24 are allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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